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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,394	09/16/2003	Yusuke Igarashi	14225-026001 / F1030478US	2925

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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,394	IGARASHI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/16/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9/16/03 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/20/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 16-18 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225

USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-18 provisionally rejected under the judicially created doctrine of double patenting over claims 1-18 of Igarashi et al., copending Application No. 10/664,209, filed Sept. 17, 2003 (U.S. Patent Appl. Pub. No. 2004/0097081), in view of Tanaka (U.S. Patent No. 5,258,649). This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

7. As to claim 1, Igarashi claims a method of manufacturing circuit devices, comprising: preparing a laminated plate by laminating a thin first conductive film and a thick second conductive film via a third conductive film (Application No. 10/664,209, page 27, lines 1-5); forming a fine conductive pattern layer by etching said first conductive film into a desirable pattern (page 27, lines 6-7); removing the third conductive film by use of said conductive pattern layer as a mask and thus forming anchor portions where said third conductive film is depressed further inside than said

conductive pattern layer (page 27, lines 8-11); fixedly fitting semiconductor elements on said conductive pattern layer (page 27, lines 12-13); electrically connecting electrodes of said semiconductor elements with predetermined parts of said conductive pattern layer (page 27, lines 14-16); covering said semiconductor elements with a sealing resin layer and filling said sealing resin layer into said anchor portions (page 27, lines 17-19); and exposing said sealing resin layer and said third conductive film on the rear surface by removing said second conductive film (page 28, lines 1-3).

8. Igarashi does not expressly claim fixedly fitting semiconductor elements on said conductive pattern layer, via an insulating adhesive layer and filling said insulating adhesive layer into said anchor portions. Tanaka teaches the general concept of anchoring an element to a package structure, by forming adhesive layer (8) such that it interlocks with concave portions (5b) of element (5) (column 14, lines 56-63; Figure 13). Moreover, Tanaka teaches, anchoring is essential in preventing element (5) from separating from the package structure (column 14, lines 59-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fit semiconductor elements on said conductive pattern layer, via an insulating adhesive layer and filling said insulating adhesive layer into said anchor portions. One who is skilled in the art would be motivated to prevent the semiconductor element from separating from the conductive pattern layer.

9. As to claim 2, Igarashi claims that the third conductive film is used as an etching stopper when the first conductive film is etched (page 28, lines 4-6).

10. As to claim 3, Igarashi claims that a solution containing ferric chloride or cupric chloride is used as a solution to perform said etching (page 28, lines 7-9).

11. As to claim 4, Igarashi claims that said anchor portions are formed by overetching said third conductive film by use of said conductive pattern layer or a resist for forming said conducive pattern as a mask (page 28, lines 10-12).

12. As to claim 5, Igarashi claims that the etching solution is an iodine-based solution (page 28, lines 13-14).

13. As to claim 6, Igarashi claims that the third conductive film is peeled off by electrolysis by use of said conductive pattern layer or a resist for forming said conducive pattern as a mask, and said anchor portions are formed by over-peeling (page 28, lines 15-18).

14. As to claim 7, Igarashi claims that the third conductive film and said sealing resin layer in said anchor portions remaining after entirely etching the second conductive film are exposed (page 28, lines 19-22).

15. As to claim 8, Igarashi claims that the external electrodes are formed by adhering a brazing filler material to the remaining third conductive film (page 29, lines 1-3).

16. As to claim 9, Igarashi claims a method of manufacturing circuit devices, comprising: preparing a laminated plate by laminating a thin first conductive film and a thick second conductive film via a third conductive film (page 29, lines 4-8); selectively forming pads formed of a fourth conductive film on said first conductive film (page 29, lines 9-10); forming a fine conductive pattern layer by etching said first conductive film into a desirable pattern (page 29, lines 11-12); removing said third conductive film by

use of the conductive pattern layer as a mask and thus forming anchor portions where said third conductive film is depressed further inside than said conductive pattern layer (page 29, lines 13-16); fixedly fitting semiconductor elements on said conductive pattern layer (page 29, lines 17-18); electrically connecting electrodes of said semiconductor elements with said pads on predetermined parts of said conductive pattern layer (page 29, lines 19-21); covering said semiconductor elements with a sealing resin layer and filling said sealing resin layer into the anchor portions (page 30, lines 1-3); and exposing said sealing resin layer and third conductive film on the rear surface by removing said second conductive film (page 30, lines 4-6).

17. Igarashi does not expressly claim fixedly fitting semiconductor elements on said conductive pattern layer, via an insulating adhesive layer and filling said insulating adhesive layer into said anchor portions. Tanaka teaches the general concept of anchoring an element to a package structure, by forming adhesive layer (8) such that it interlocks with concave portions (5b) of element (5) (column 14, lines 56-63; Figure 13). Moreover, Tanaka teaches, anchoring is essential in preventing element (5) from separating from the package structure (column 14, lines 59-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fit semiconductor elements on said conductive pattern layer, via an insulating adhesive layer and filling said insulating adhesive layer into said anchor portions. One who is skilled in the art would be motivated to prevent the semiconductor element from separating from the conductive pattern layer.

18. As to claim 10, Igarashi claims that the third conductive film is used as an etching stopper when the first conductive film is etched (page 30, lines 7-9).

19. As to claim 11, Igarashi claims that a solution containing ferric chloride or cupric chloride is used as a solution to perform said etching (page 30, lines 10-12).

20. As to claim 12, Igarashi claims that the anchor portions are formed by overetching said third conductive film by use of said conductive pattern layer or a resist for forming said conducive pattern as a mask (page 30, lines 13-15).

21. As to claim 13, Igarashi claims that the etching solution is an iodine-based solution (page 30, lines 16-17).

22. As to claim 14, Igarashi claims that the third conductive film is peeled off by electrolysis by use of said conductive pattern layer or a resist for forming said conducive pattern as a mask, and said anchor portions are formed by over-peeling (page 30, lines 18-21).

23. As to claim 15, Igarashi claims that third conductive film and said sealing resin layer in said anchor portions remaining after entirely etching the second conductive film are exposed (page 31, lines 1-4).

24. As to claim 16, Igarashi claims that external electrodes are formed by adhering a brazing filler material to the remaining third conductive film (page 31, lines 5-7).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yagi et al. (U.S. Patent No. 6,133,070) discloses forming a

circuit member with laminated metal layers and encasing the semiconductor element in an epoxy resin. Omote et al. (U.S. Patent No. 6,096,482) discloses forming a circuit substrate with metal and resin layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC
May 6, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER